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S145AST M/B Schematics Document


REV : 0 . 2

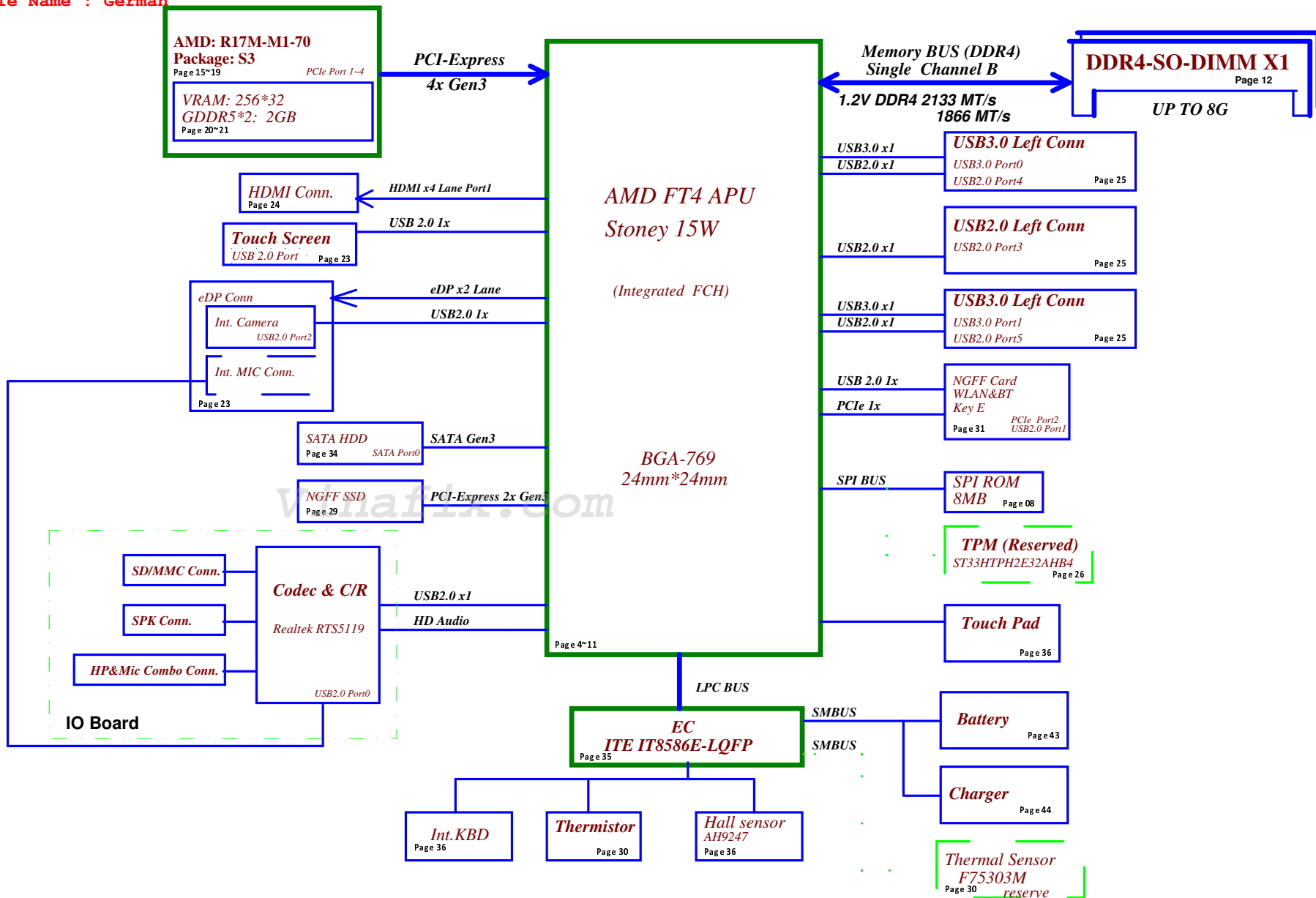
AMD FT4 Stoney SOC with DDRIV

AMD R17M-M1-70

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2018-10

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Voltage Rails (O --> Means ON , X --> Means OFF)

power plane	B+ (+20VSB)	+5VALW (+3VALW_APU)	+2.5V (+VSYSMEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.6VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
State	+3VL +5VLP	+1.8VALW +0.95VALW +0.775VALW		
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

BOARD Config.	BOARD_ID1	BOARD_ID2 reserve
	0: Dis	0: No KBL
	1: UMA	1: KBL

BOARD Config.	BOARD_ID0	BOARD_ID3
14''	0	0
15''	0	1
17''	1	0

USB Port Table for Stoney FT4

USB 2.0	USB 3.0	Port	Port device
EHCI		0	Card Reader
		1	Blue Tooth
		2	Camera
		3	LEFT USB (2.0)
xHCI		4	LEFT USB (3.0) Lower
		5	LEFT USB (3.0) upper
		6	Touch screen
		7	

PCIE PORT LIST

	Port	Device
GPP	0	SSD
	1	
	2	WLAN
	3	N/A
GFX	0	
	1	DIS GPU
	2	
	3	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
Debug@	For USB debug part
NODebug@	For USB no debug part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_PX@	EMC GPU part
EMC_PXNS@	EMC GPU reserve part
RF_NS@	RF reserve Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
AOAC@	AOAC support part
HDT@	HDT Debug part
TS@	Touch screen part
NOTS@	No Touch screen part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2GX4@	X76 SAMSUNG 1G
M2GX4@	X76 MICRON 1G
H2GX4@	X76 HYNIX 1G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
S1G@	SAMSUNG 1G
M1G@	MICRON 1G
H1G@	HYNIX 1G
SIVCD@	SIV COST down material
HDMI@	HDMI Logo
STN@	Stoney part

VRAM

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586E	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	X	V		X	X	X	X	V	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V	X		X	X	V	V	X	X	X
APU_SMB_CLK APU_SMB_DATA	APU +3VS	X	X	X	V	V	X		X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VL_EC	X	X		X	X	X	X	X	V	X
TP_I2C0_SCL_R TP_I2C0_SDA_R	APU +1.8VS	X	X	X	X	X	X		X	X	V

EC SM Bus1 address EC SM Bus2 address EC SM Bus3 address

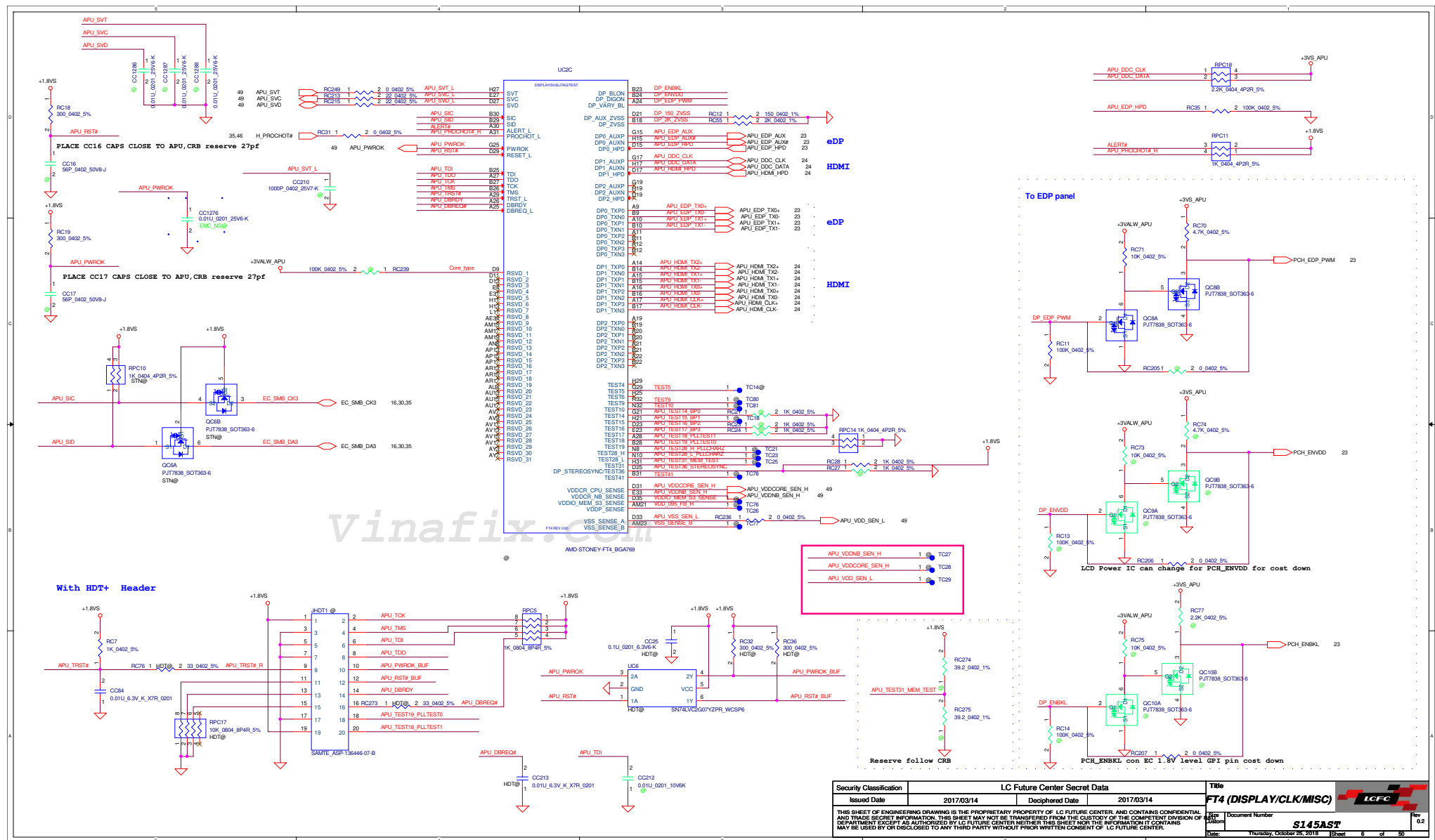
Device	Address	Device	Address	Device	Address
Battery	0X16	PMIC	0X34	Thermal Sensor	1001_100xb(reserve)
Charger	0001 0010 b			GPU	0x41(default)
				APU SB-TSI	relate to F3x1E4[SblAddr] or Address Select Pins setting

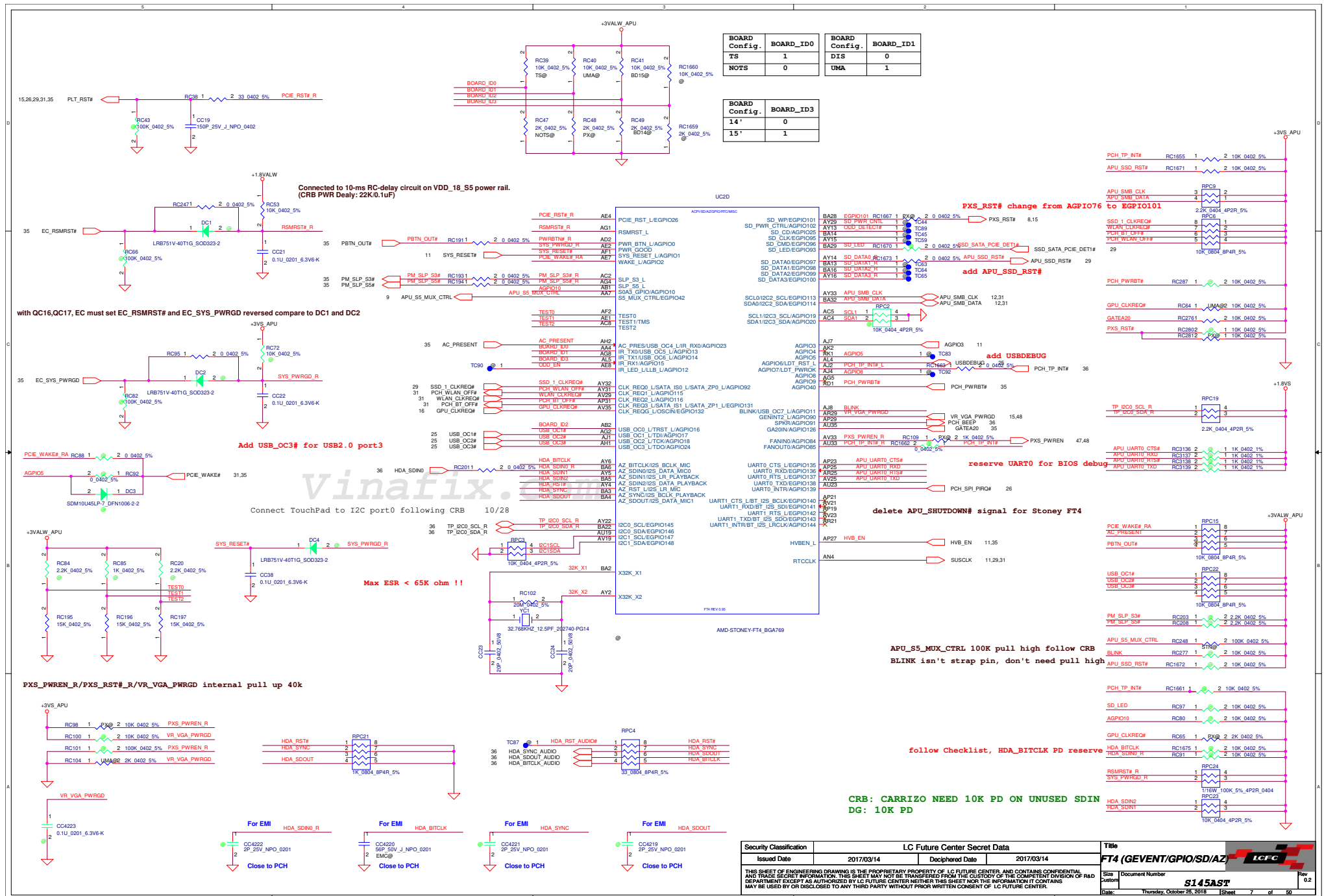
APU SM Bus1 address APU SM Bus2 APU SM Bus3 address APU SM Bus4

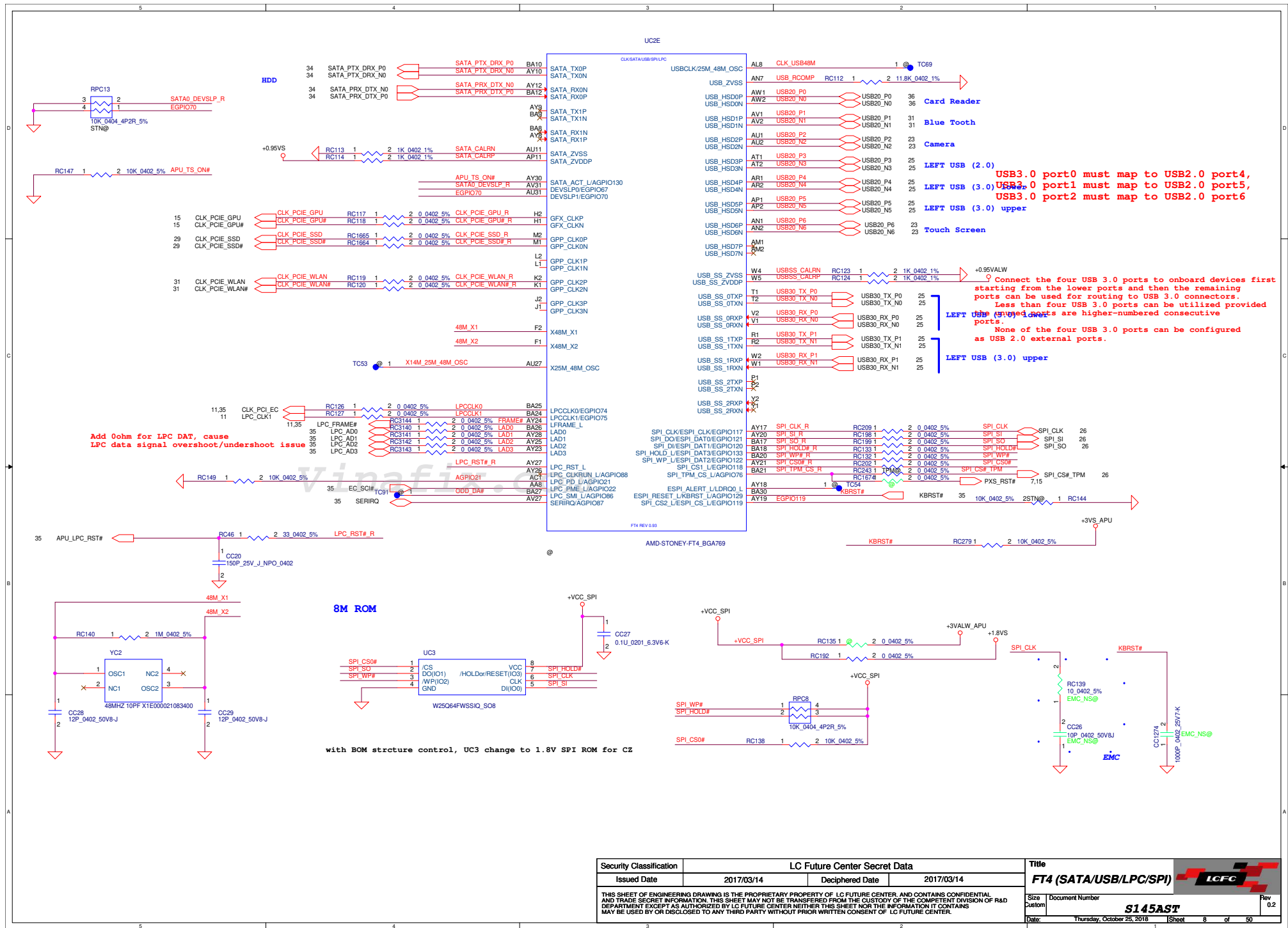
Device	Address	Device	Address
Touch pad	0x15	No use	No use
		DDR DIMM	0xA0h
		WLAN	RSVD

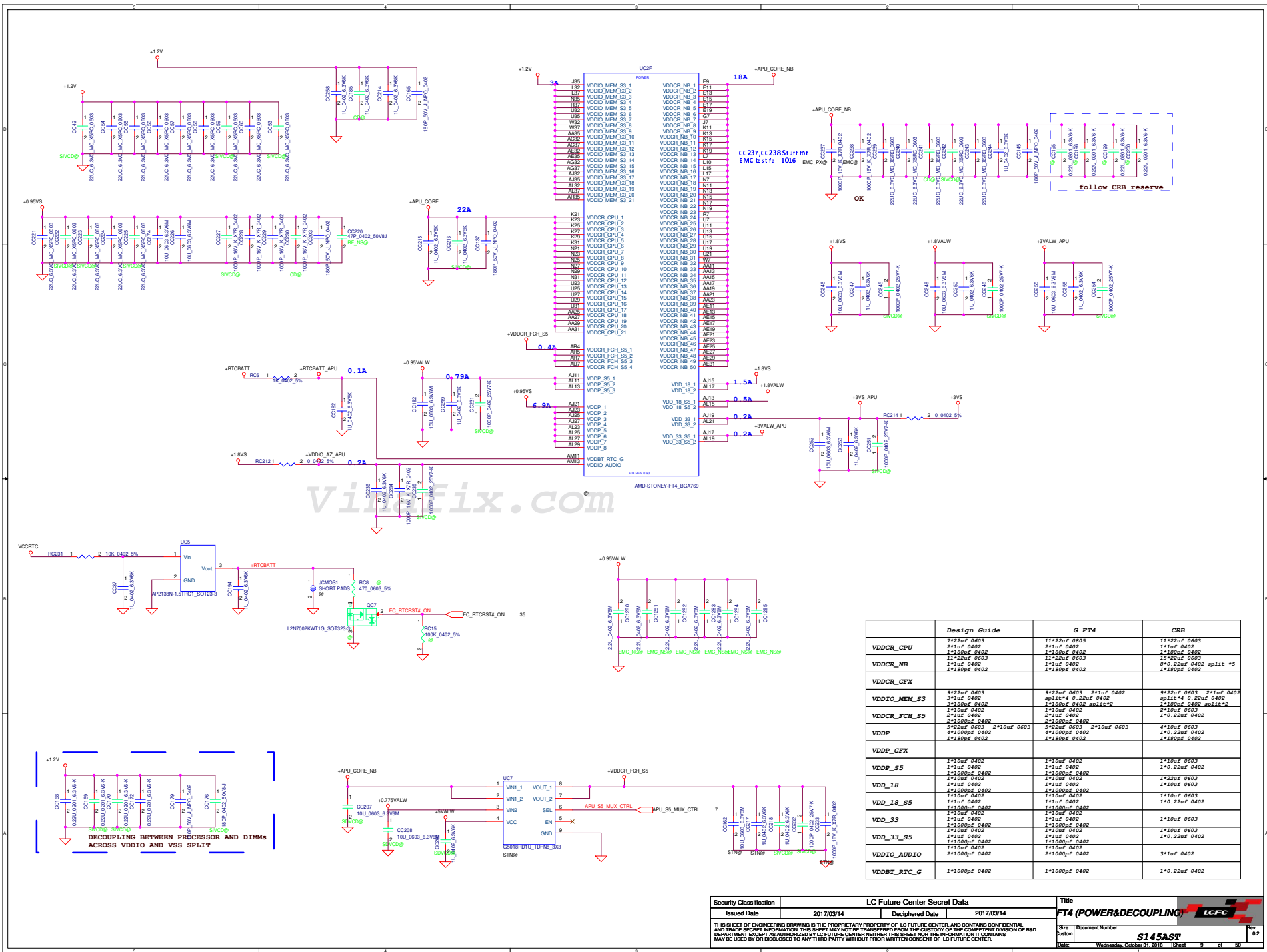
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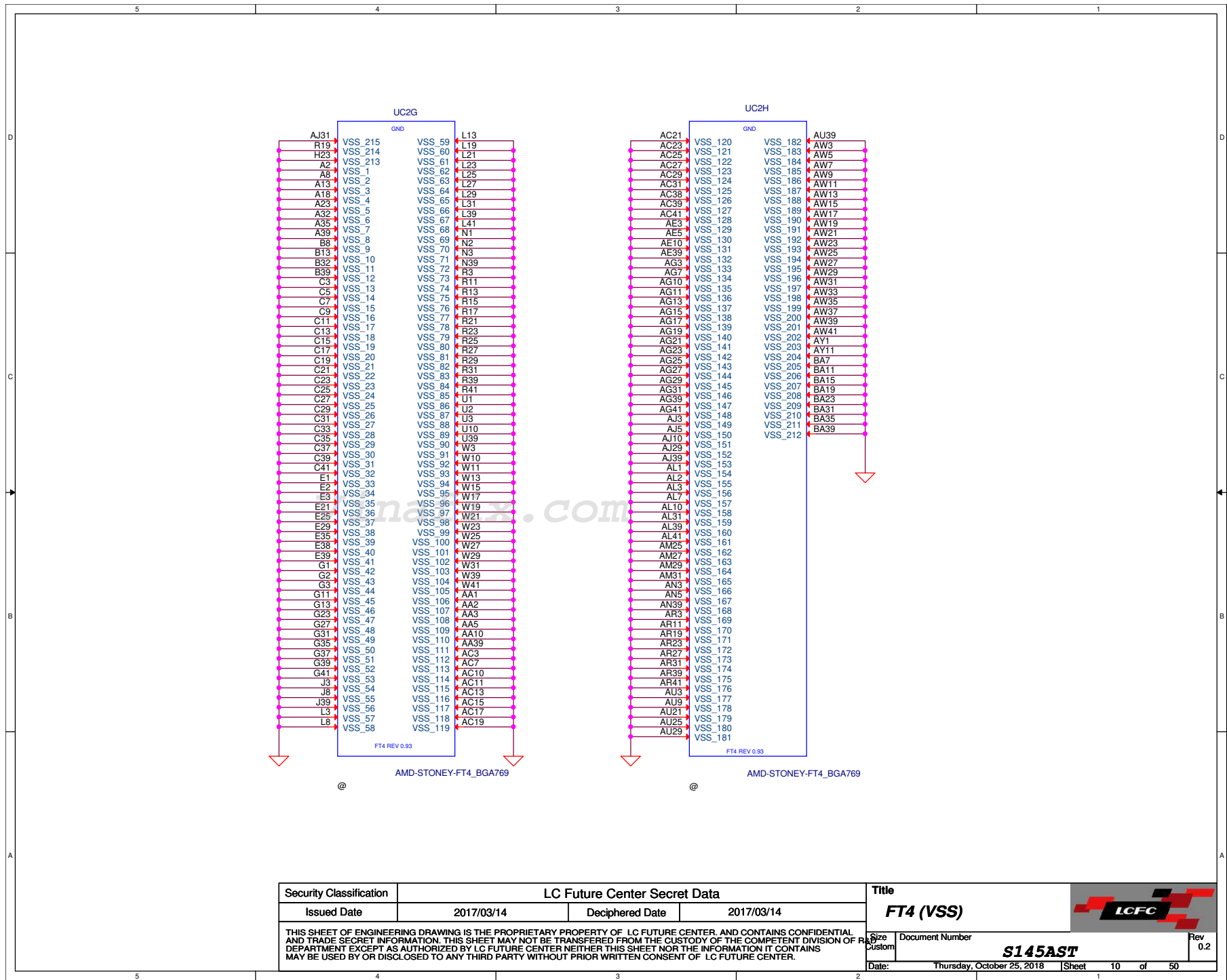
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The diagram illustrates the electrical connections for a DDR4 SO-DIMM A module. It includes a detailed pinout for the DIMM, showing connections for data signals (DQ, DQS, DQSI, DQSI#), address signals (A0-A15), command signals (C0-C3), and various control signals (B0-B7, CS0-CS3, ODT0-ODT3, VREF, etc.). The schematic also shows the internal structure of the DIMM, including the memory array, sense amplifiers, and control logic. Key components like capacitors (CD1, CD2, etc.) and resistors (RD1, RD2, etc.) are shown with their values and placement notes. A layout note specifies the placement of capacitors near the DIMM pins to ensure proper signal integrity. The diagram is labeled 'DDR4 SO-DIMM A' and includes a title block with the document number 'S145AST' and the date 'Thursday, October 25, 2018'.

SPD Address = A0H

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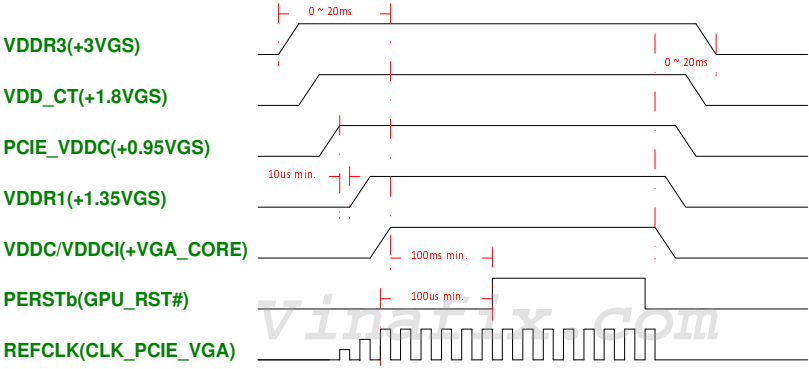
Power-Up/Down Sequence

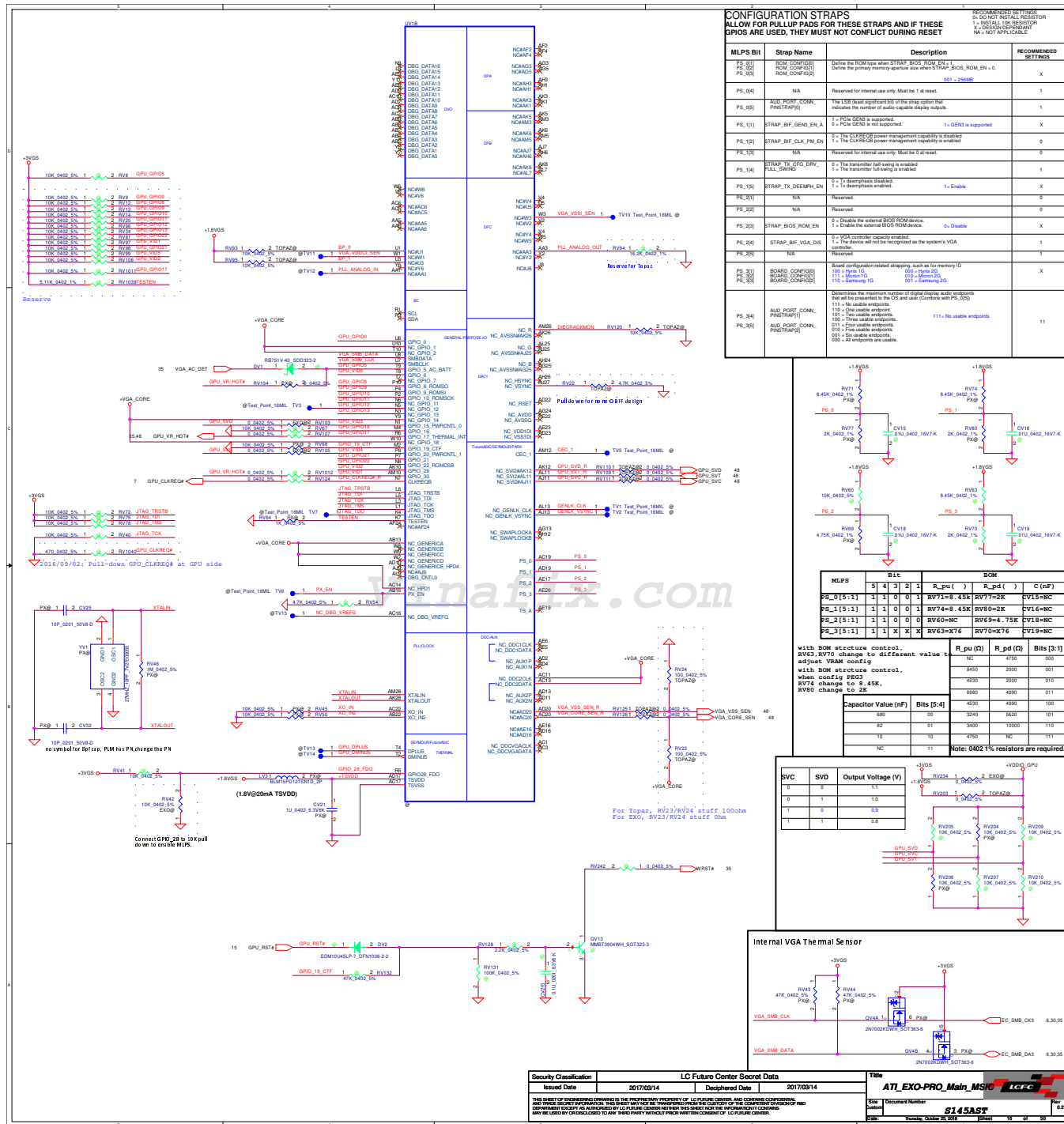
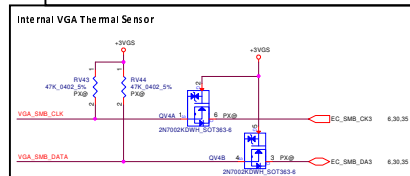
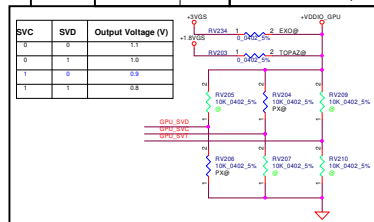
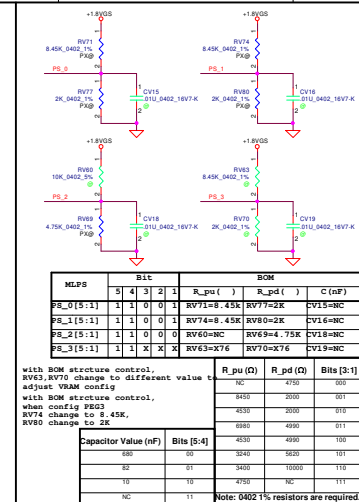
"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:


All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
It is recommended that the 3.3-V rail ramp up first.
The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up.
The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μs).
For power down, reversing the ramp-up sequence is recommended.

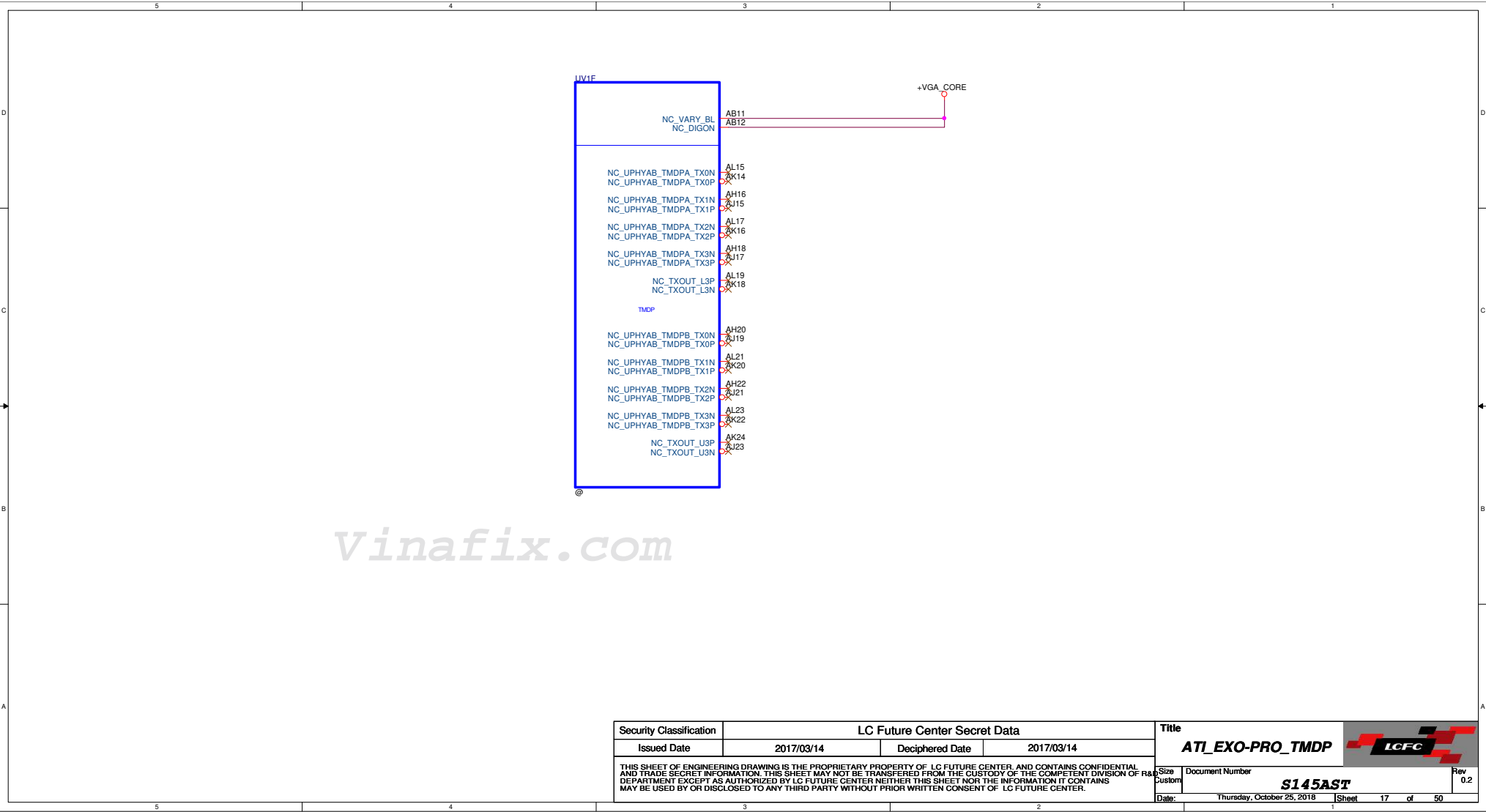
VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
256Mx32	Hynix H5GC8H24AJR-R0C 6.0Gbps@1.35V	100	4.53K	4.99K
	Micron MT51J256M32HF-70:B 6.0Gbps@1.35V	111	4.75K	NC
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	110	3.4K	10K




[illegible]


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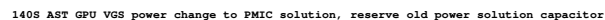


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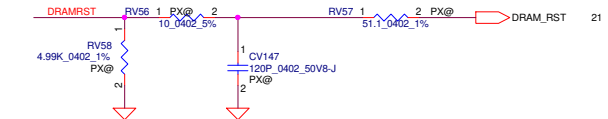
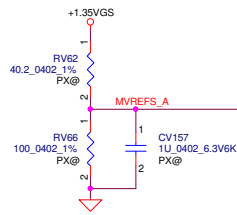
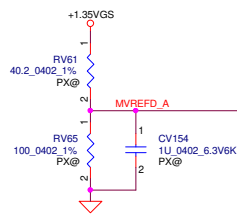
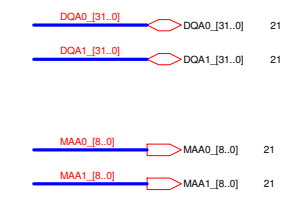
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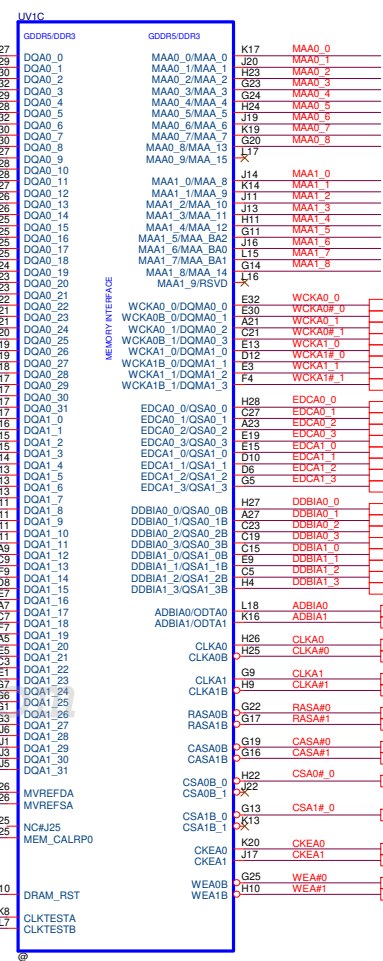
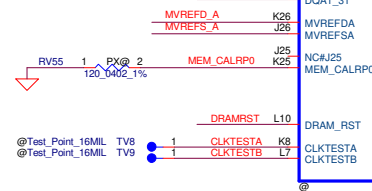
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The schematic diagram illustrates the PCH_ENVDD power supply circuit. A 3VS input is connected to a 1uF capacitor and the IN pin of a SY6288C20AAC voltage regulator (U7). The regulator's EN pin is connected to a PCH_ENVDD signal. The output of the regulator is connected to the PCH_ENVDD signal line through a 100K resistor. The regulator's GND and OCB pins are connected to ground.

The schematic shows the PCH_ENBKL pin connected to a 3V3 supply via a 4.7K resistor (R10). It is also connected to a BKOFF# signal through a 0.0402 5% resistor (R12) and to an ENBKL signal through a 0.0402 5% resistor (R14). A 100K 0.0402 5% resistor (R16) is connected to ground.

V20B+

2A 80 mil

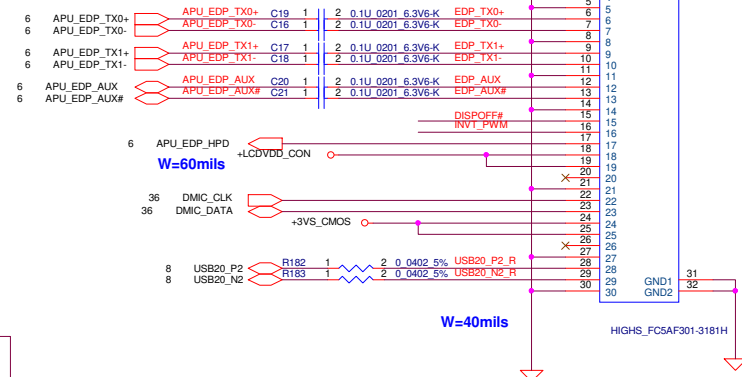
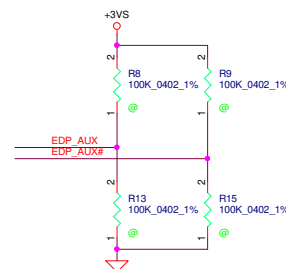
R22 1 2 0 0805 5%

+LEDVDD

F2
3A_32V_0497003PRRH#

F2 change to SP040004S00

Timing diagram for EXC24CH900U_4P showing the relationship between USB20_P2, USB20_P2_R, DMIC_CLK, DISOFF#, and INVT_PWM signals. The diagram illustrates the timing of these signals relative to a common clock or reference signal.

[illegible]

HIGHS FC5AF301-3181H

USB20_P6_CONN

USB20_N6_CONN

+5VS_TS

D2

R2

AZ5255-01F-R7GR_DF1006P2X2

EMC_NS@

D753

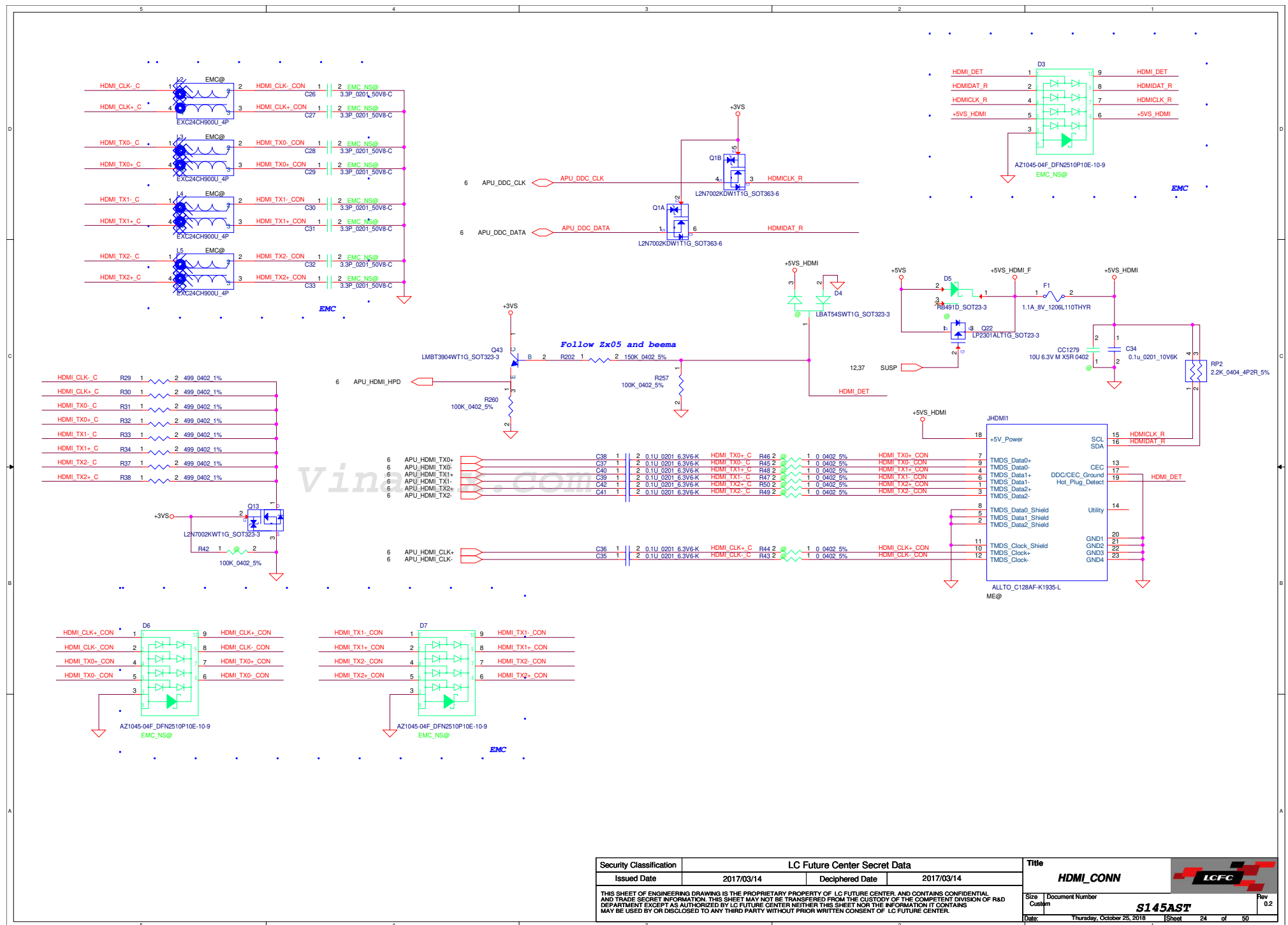
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EMC_NS@

For ESD

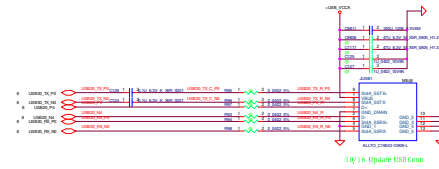
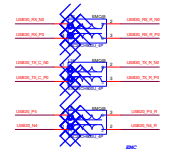


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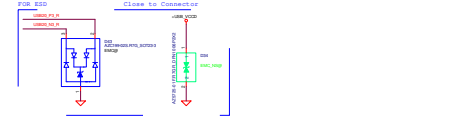
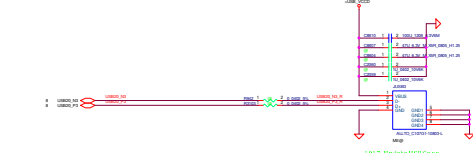
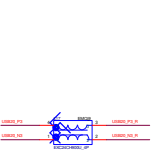


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LEFT SIDE USB3.0 PORT x2

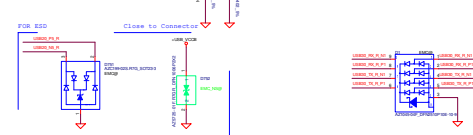
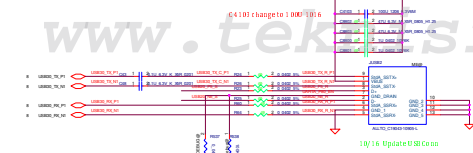
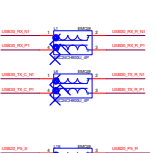


Follow S145WHL



Follow S145WHL, USB change to S4000014000

USB3.0 PORT

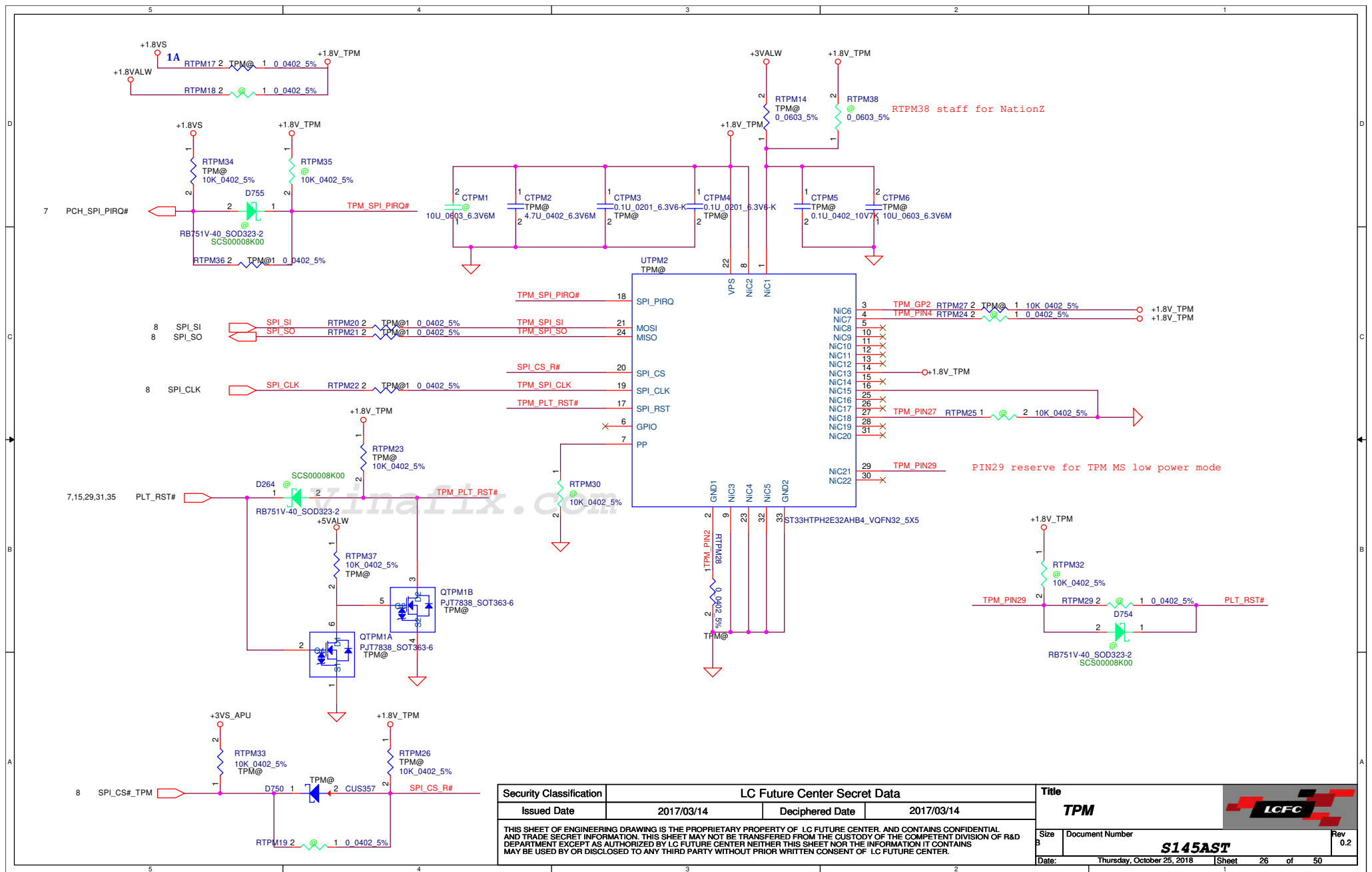


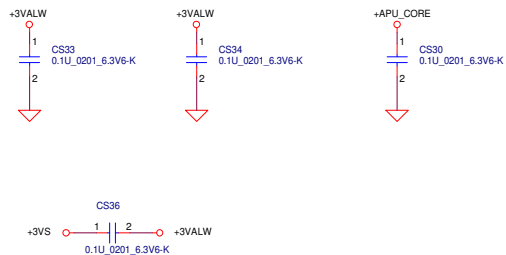
For USB Debug Function




SYMBOL	VALUE
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U2	USB3.0 PHY
U3	USB3.0 PHY
U4	USB3.0 PHY
U5	USB3.0 PHY
U6	USB3.0 PHY
U7	USB3.0 PHY
U8	USB3.0 PHY
U9	USB3.0 PHY
U10	USB3.0 PHY
U11	USB3.0 PHY
U12	USB3.0 PHY
U13	USB3.0 PHY
U14	USB3.0 PHY
U15	USB3.0 PHY
U16	USB3.0 PHY
U17	USB3.0 PHY
U18	USB3.0 PHY
U19	USB3.0 PHY
U20	USB3.0 PHY
U21	USB3.0 PHY
U22	USB3.0 PHY
U23	USB3.0 PHY
U24	USB3.0 PHY
U25	USB3.0 PHY
U26	USB3.0 PHY
U27	USB3.0 PHY
U28	USB3.0 PHY
U29	USB3.0 PHY
U30	USB3.0 PHY
U31	USB3.0 PHY
U32	USB3.0 PHY
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U39	USB3.0 PHY
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U44	USB3.0 PHY
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U48	USB3.0 PHY
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U98	USB3.0 PHY
U99	USB3.0 PHY
U100	USB3.0 PHY

SYMBOL	VALUE
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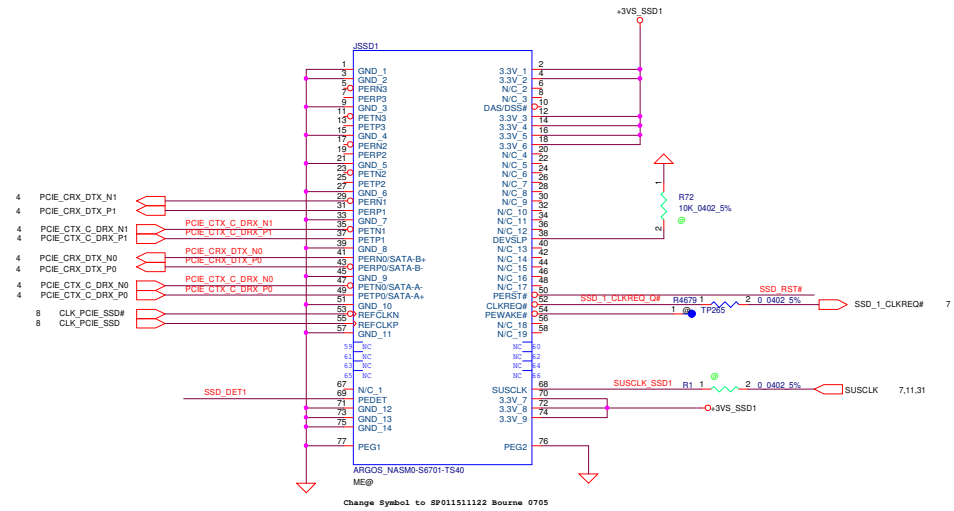
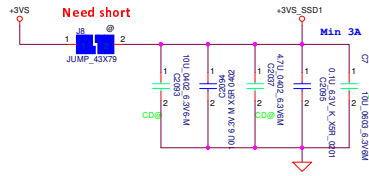


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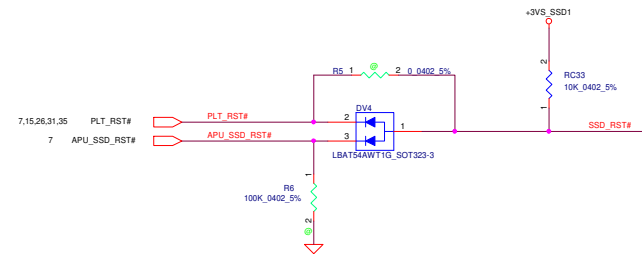
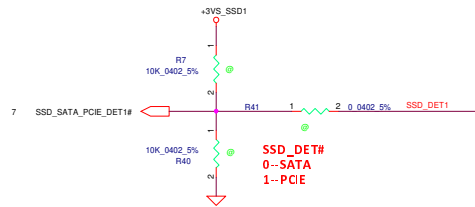
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				Date: Thursday, October 25, 2018
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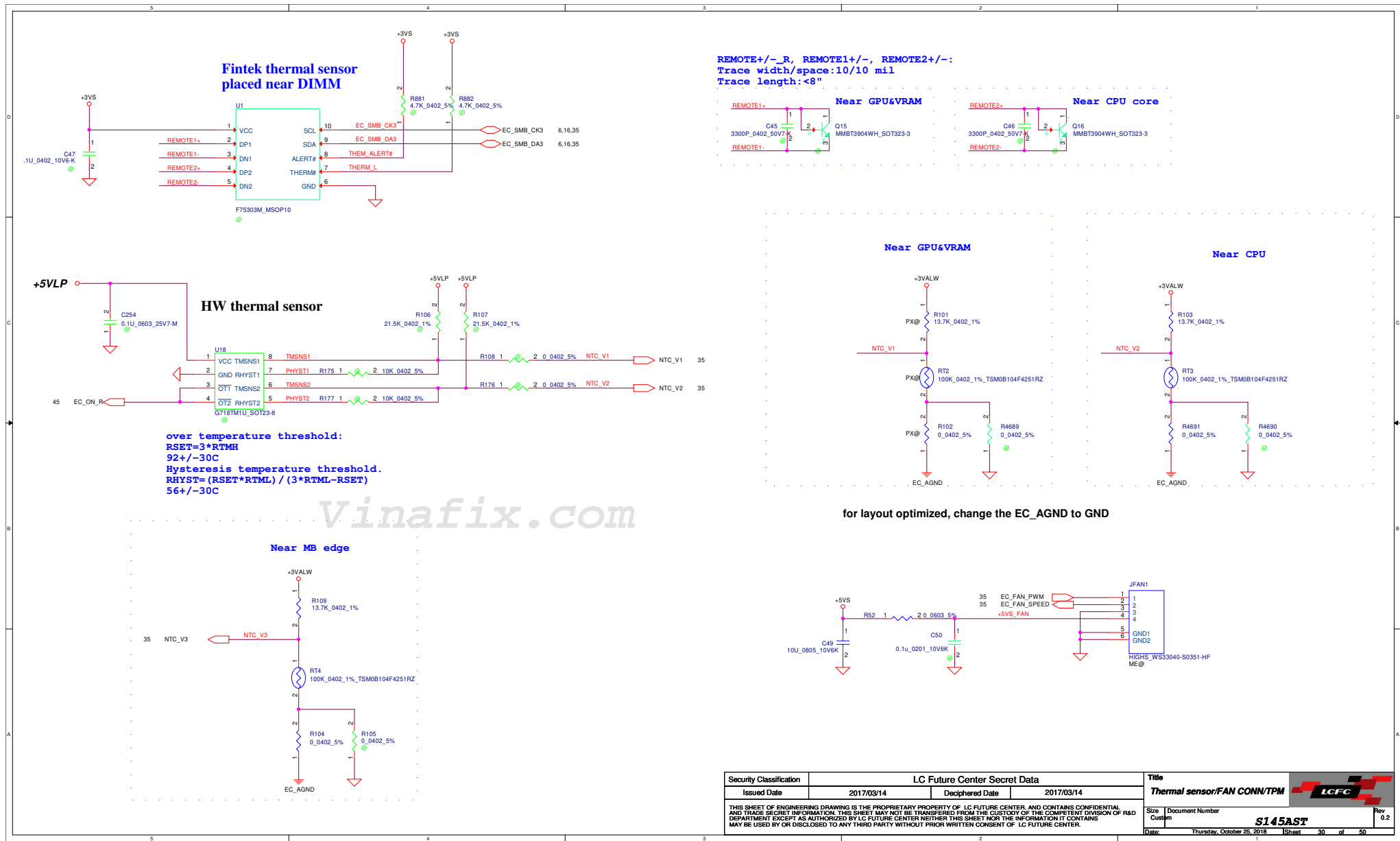
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				Custom	S145AST	0.2
				Date:	Thursday, October 25, 2018	Sheet 28 of 50



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Mini-Express Card(WLAN/WiMAX)

7 WLAN_CLKREQ# R61 2 1 0.0402 5% WLAN_CLKREQ_Q#


Not support AOAC, delete AOAC power circuit 1015

Need short


35 PWR_WLAN_EN PWR_WLAN_EN

SY6288C20AAC_SOT23-5


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Date:			Thursday, October 25, 2018	Sheet 31 of 50

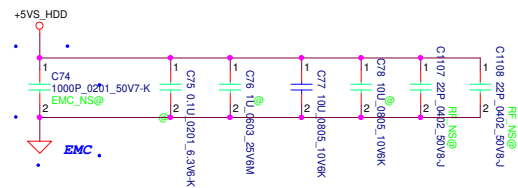
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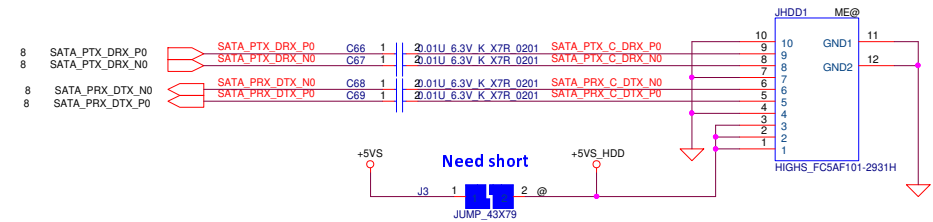
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				Date:	Thursday, October 25, 2018	Sheet	33 of 50



SATA HDD Conn.

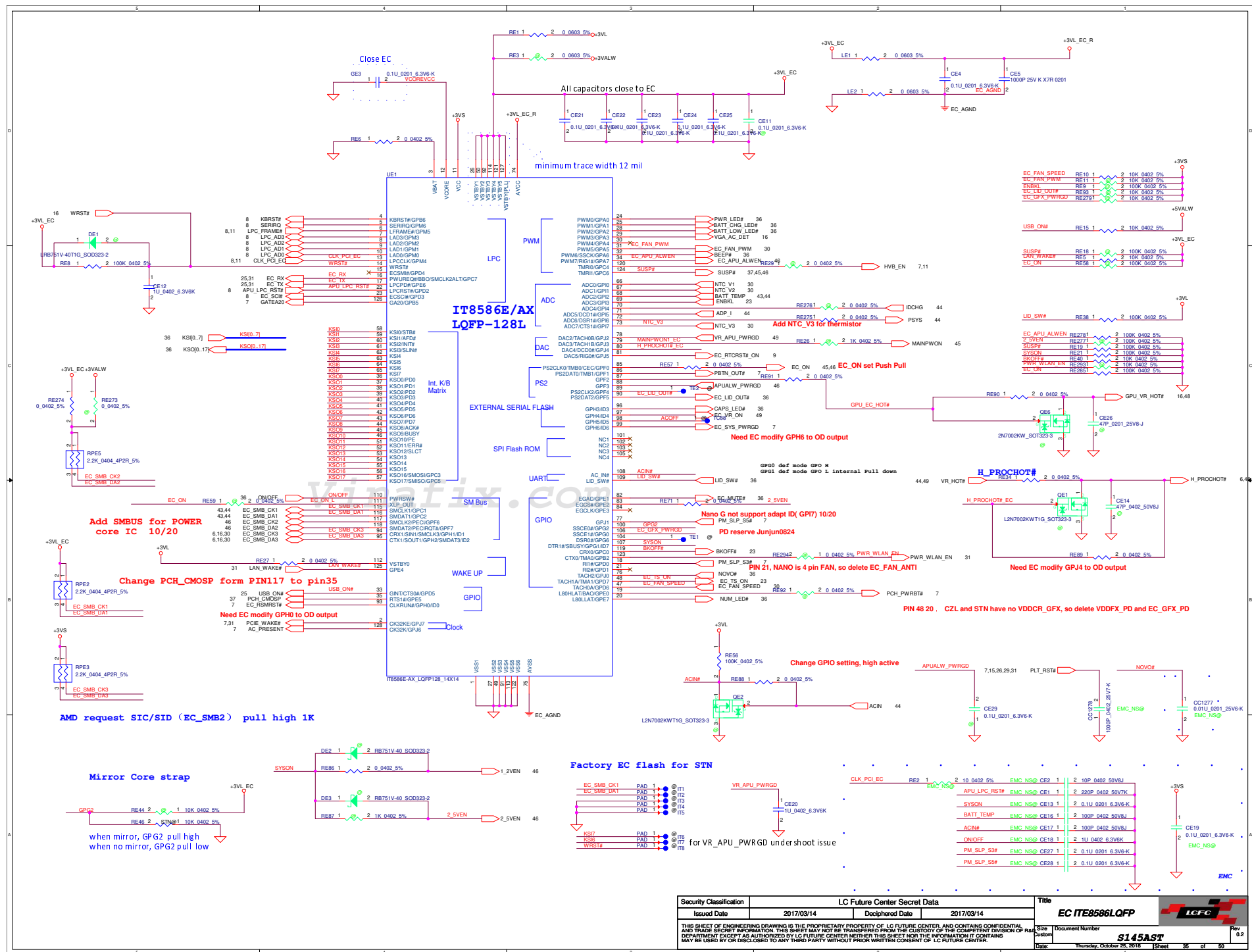


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				Date: Thursday, October 25, 2018	Sheet 34 of 50

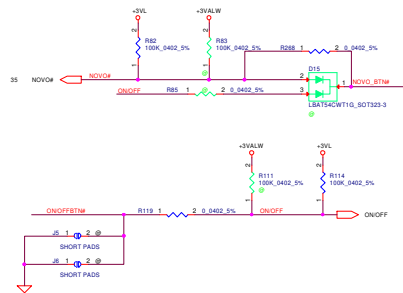


Rev 0.2

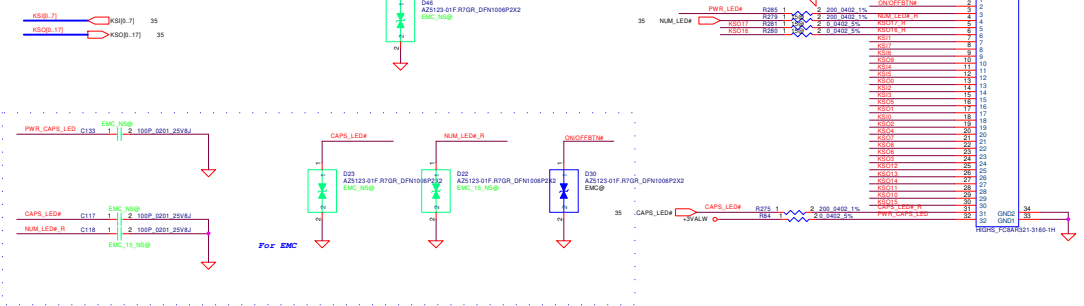


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ON/OFF switch

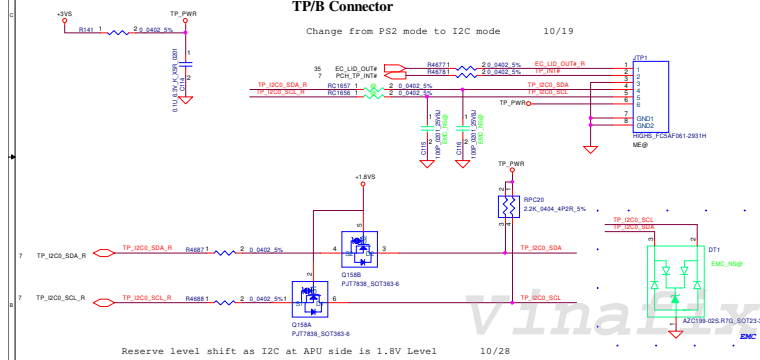


K/B Connector

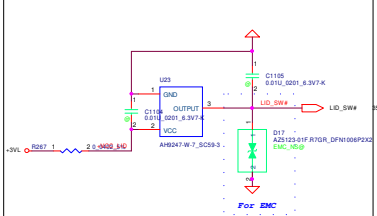


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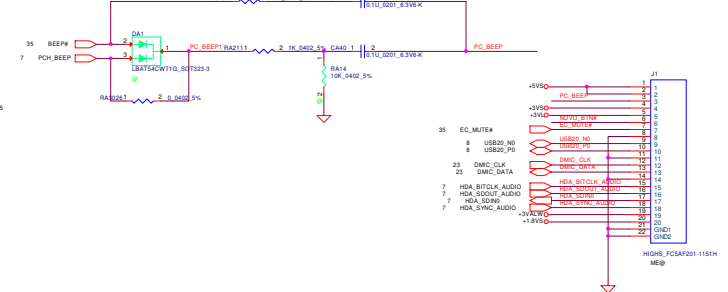
Change from PS2 mode to I2C mode 10/19



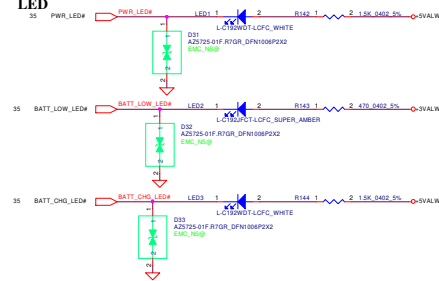
LID Connector



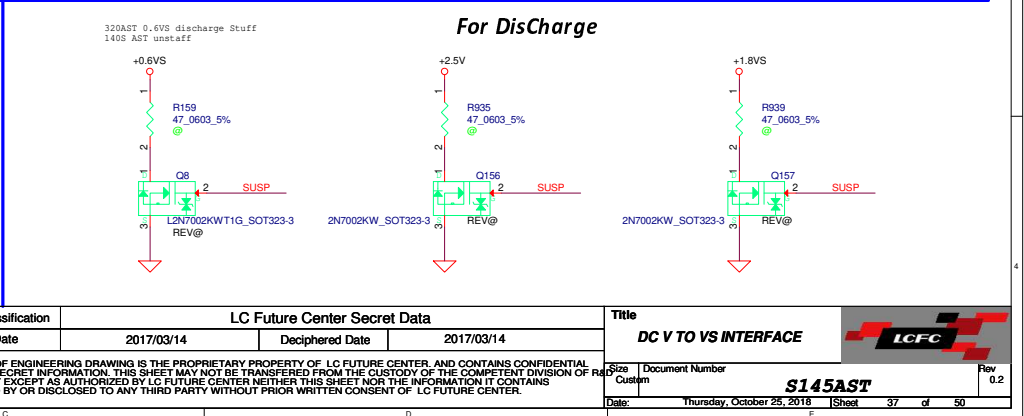
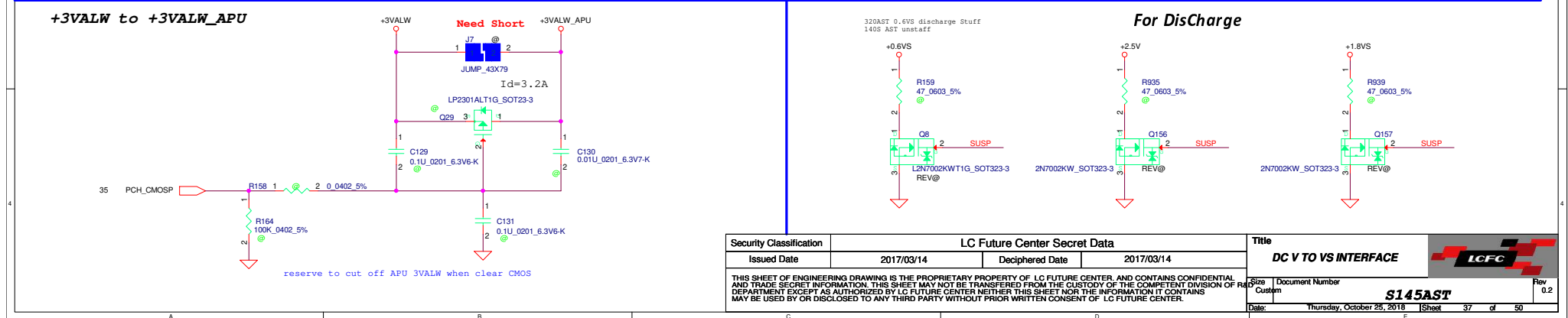
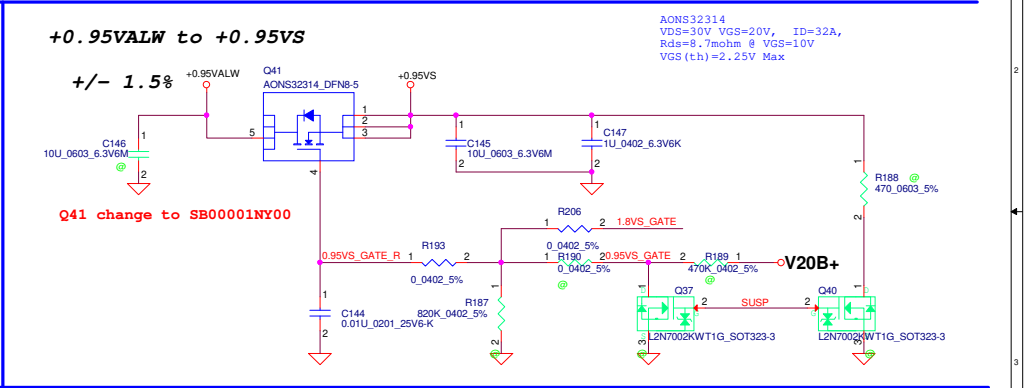
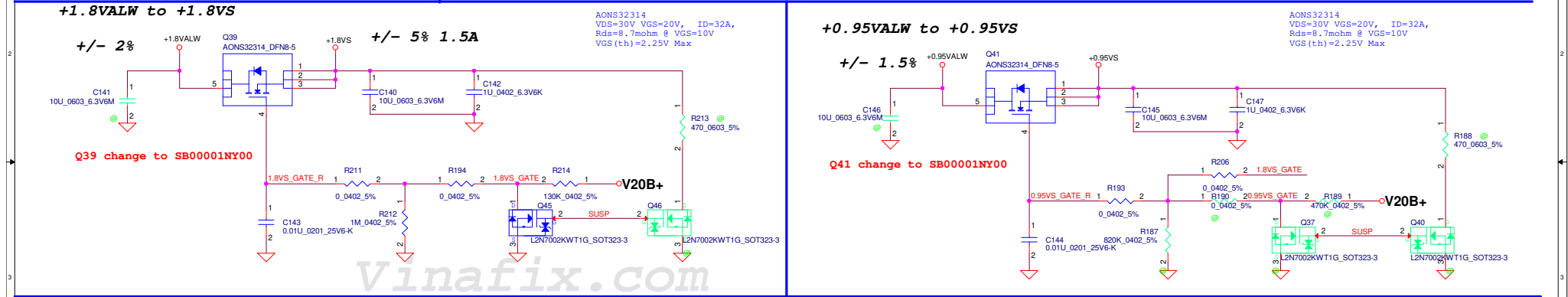
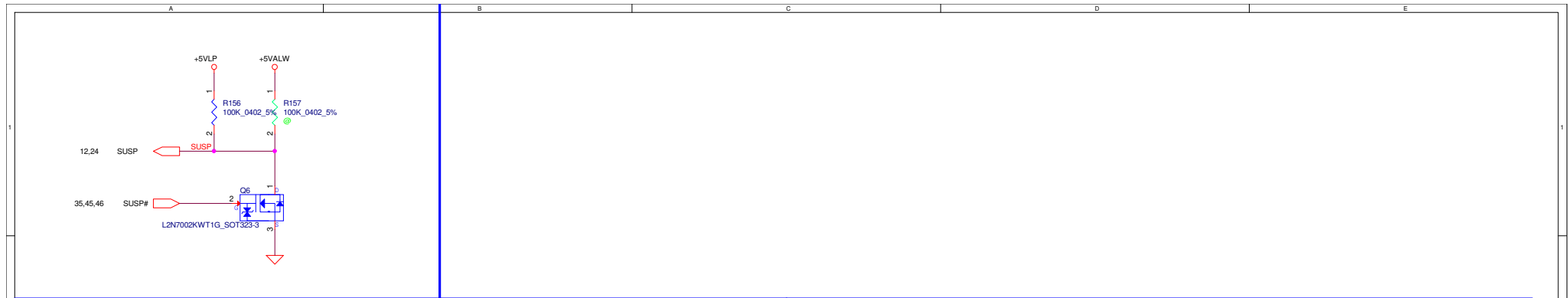
IO Connector




LED

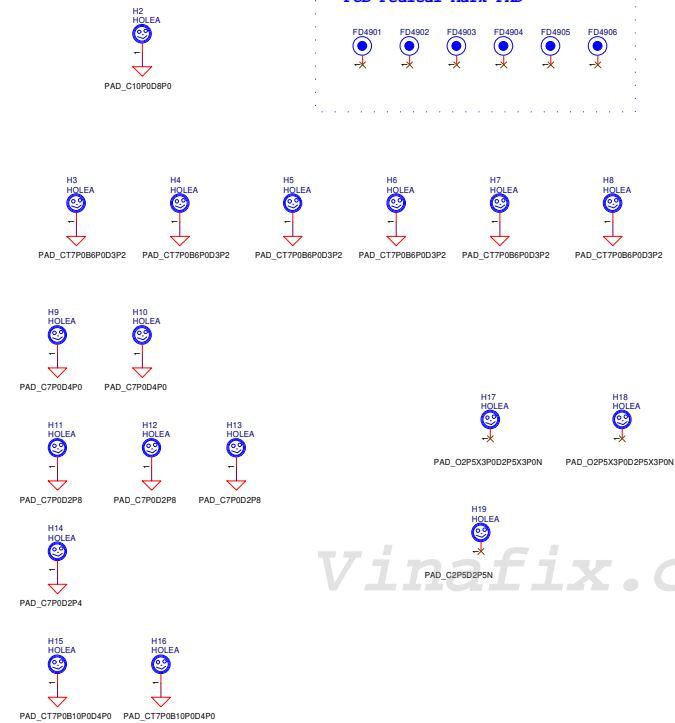


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Doc Name	KBD/PWR/IO/LED/TP Conn.		Rev
Doc Date	2017/03/14		Rev



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Date:		Thursday, October 25, 2018		Sheet		37 of 50	

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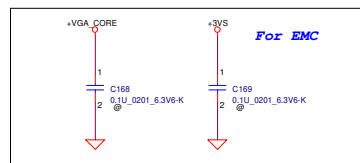
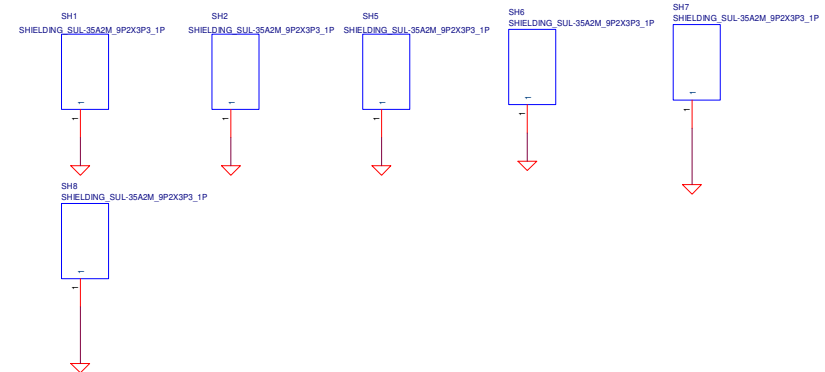


PCB Federal Mark PAD



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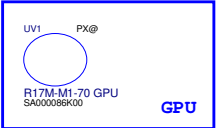
SODIMM Shielding



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Date	Thursday, October 25, 2018	Sheet	30 of 50

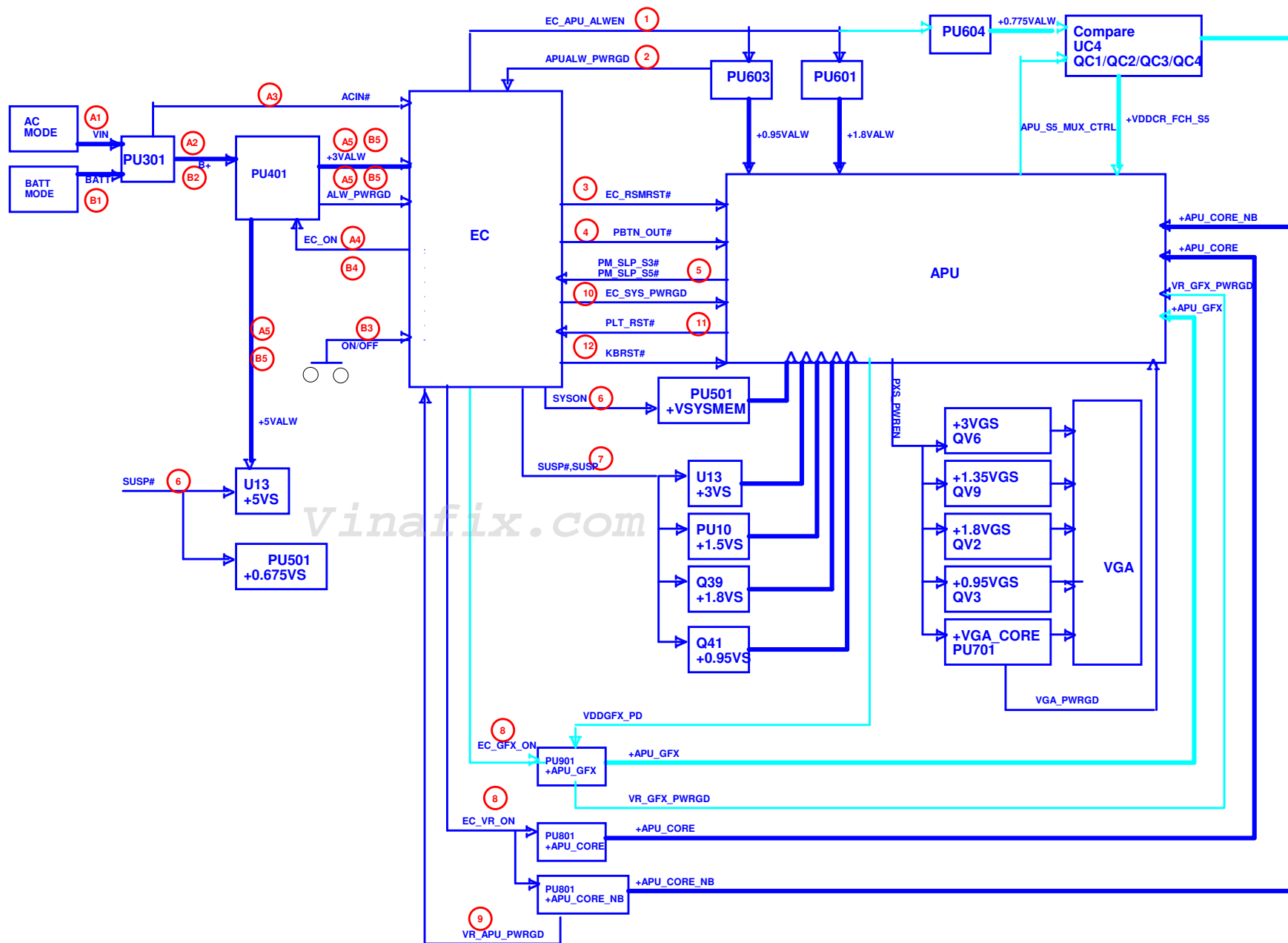


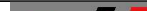
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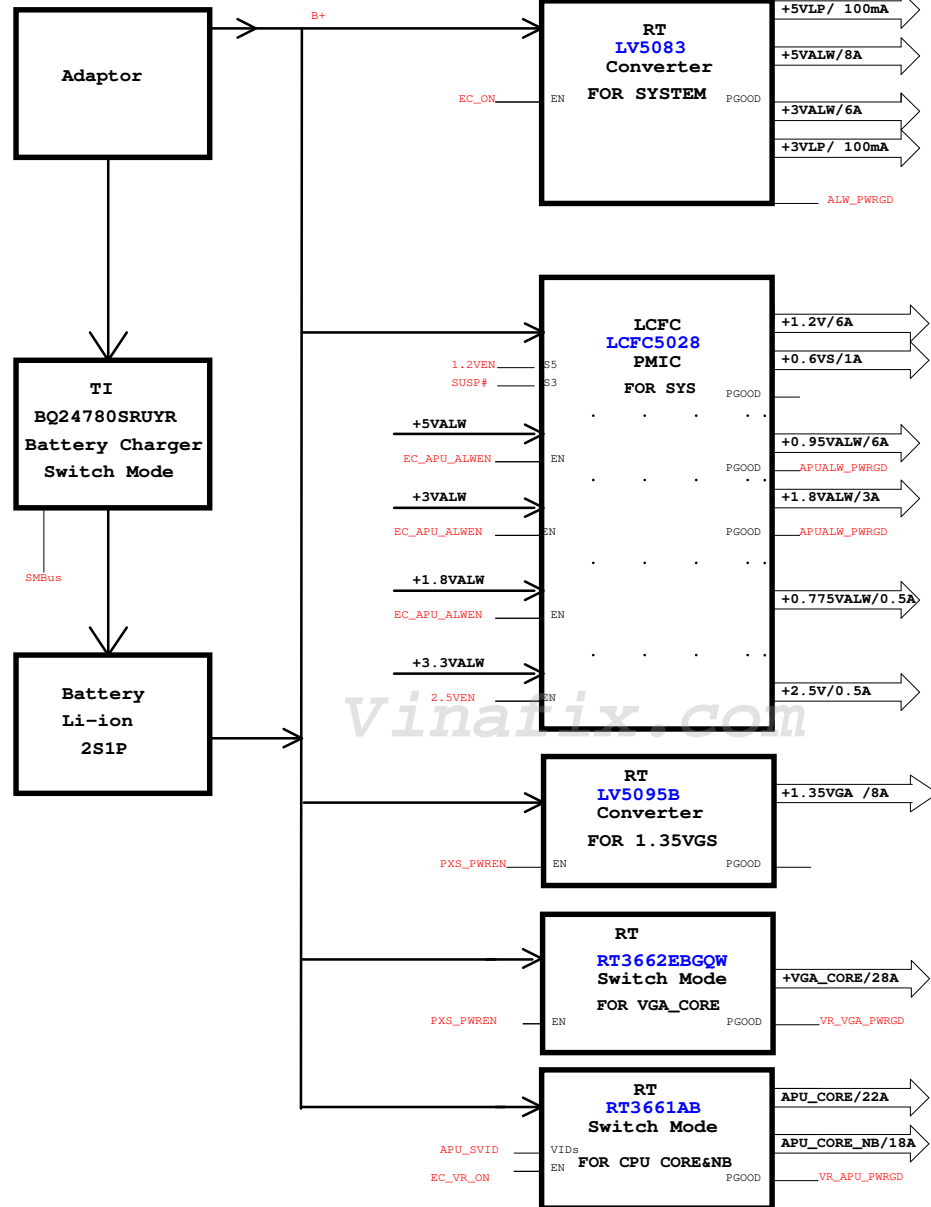
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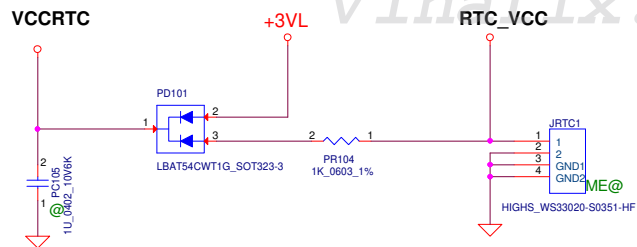
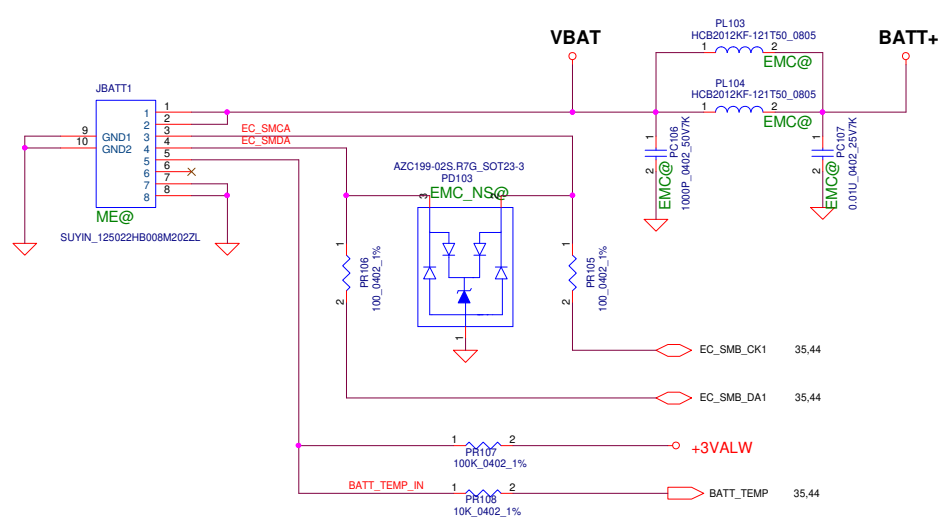
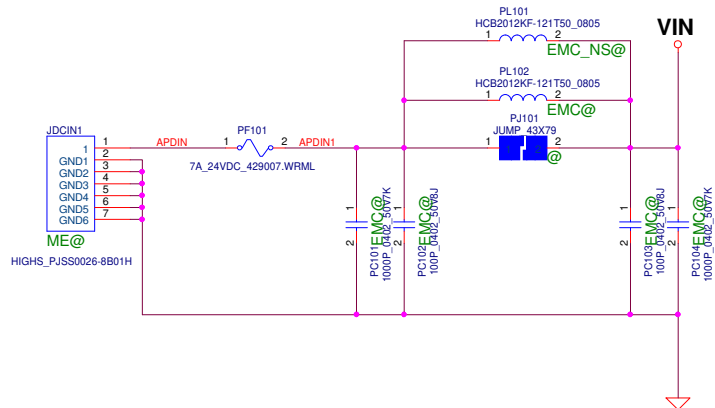


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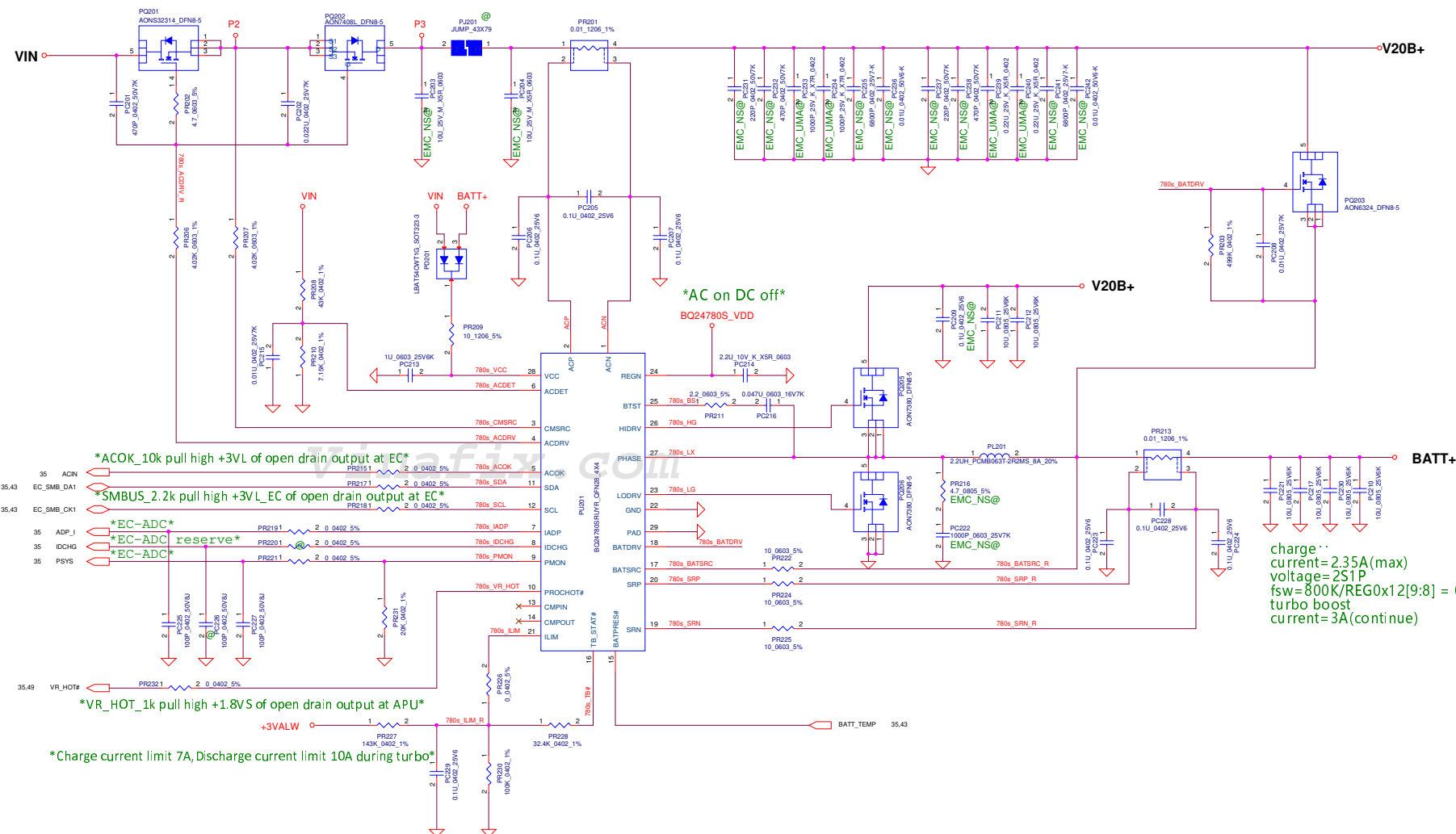
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				Date Thursday, October 26, 2018
				Sheet 41 of 50
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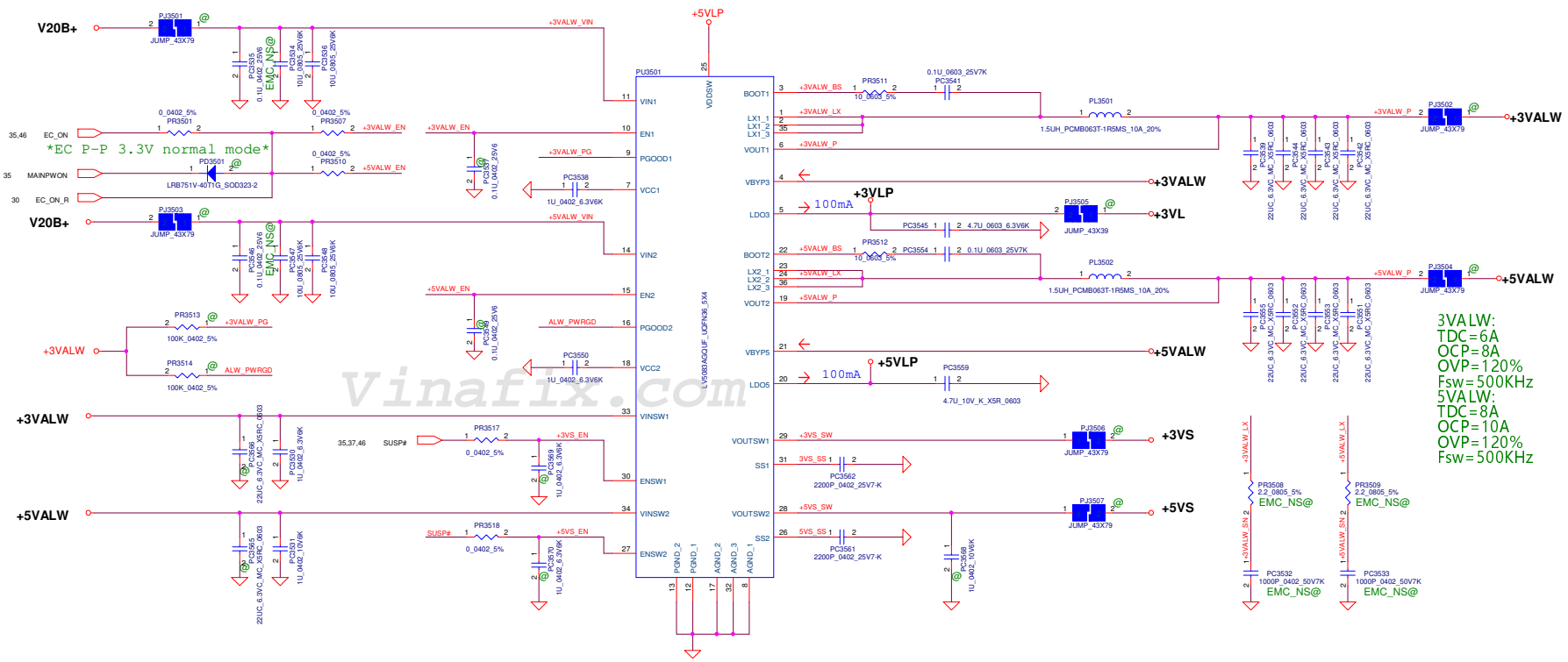



PRTC1
 BATT CR2032 3V 220MAH
 RTC@
 35mm cable
 GC02001YB00 main source
 GC02001Z800 2nd source

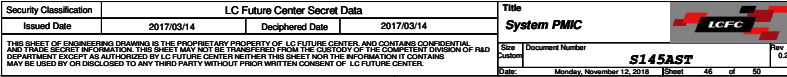
Security Classification		LC Future Center Secret Data		Title		
Issued Date	2017/03/14	Deciphered Date	2017/03/14	DCIN / RTC		
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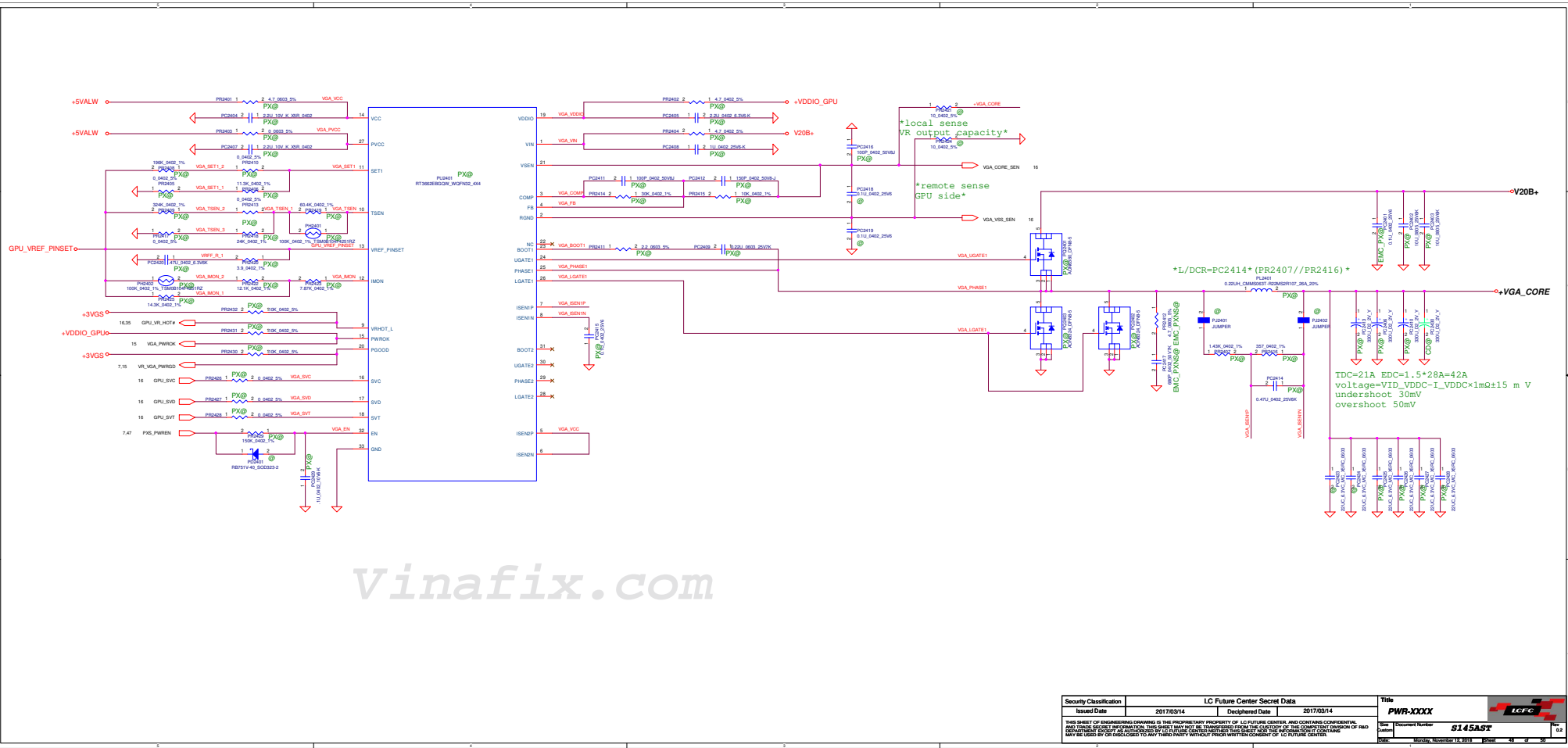
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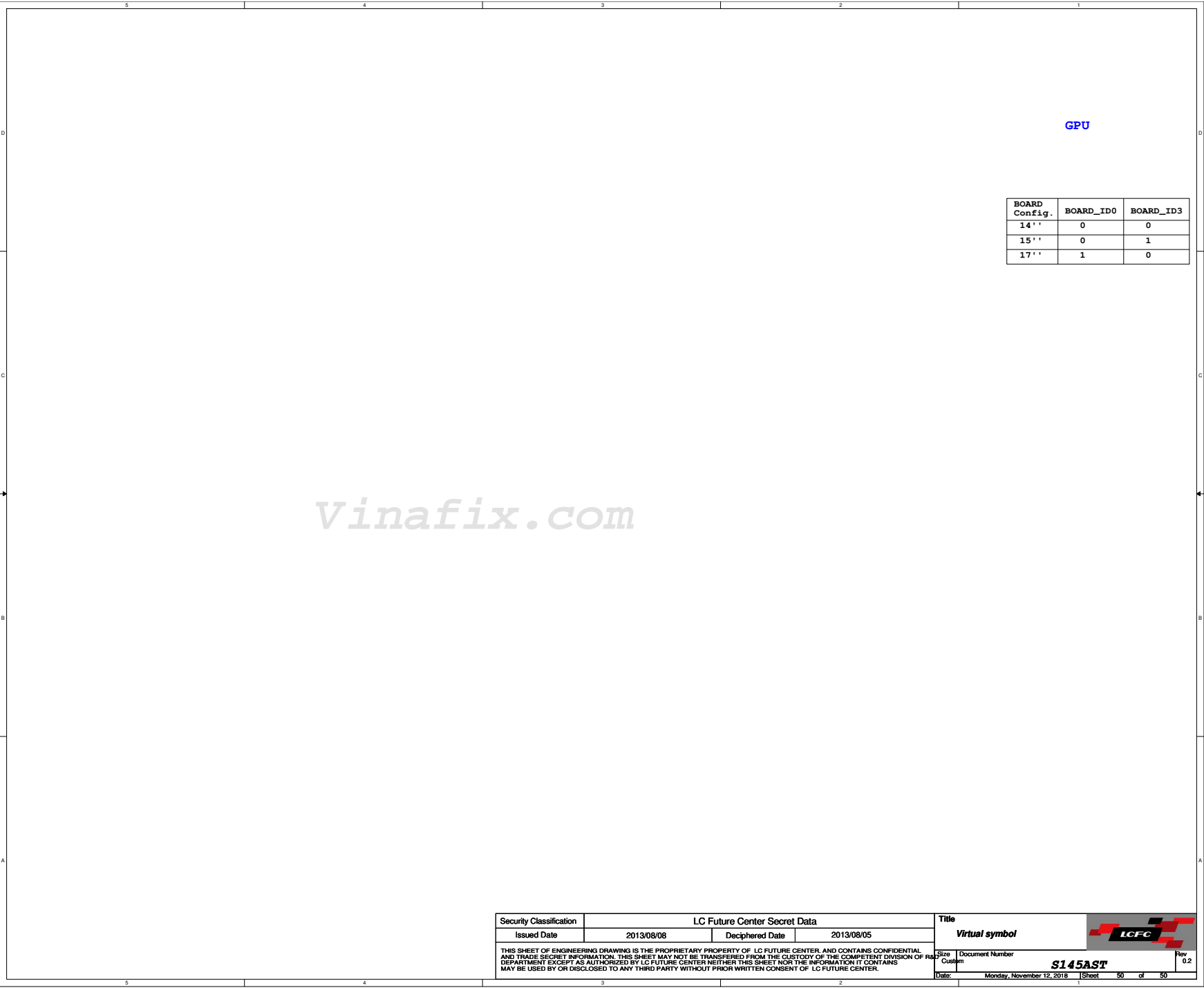


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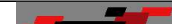


GPU

BOARD Config.	BOARD_ID0	BOARD_ID3
14''	0	0
15''	0	1
17''	1	0

Vinafix.com

Security Classification	LC Future Center Secret Data		
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Custom	S145AST	0.2
Date:	Monday, November 12, 2018	Sheet 50 of 50